



# LC72137, 72137M

## PLL Frequency Synthesizer for Electronic Tuning



### Overview

The LC72137 and LC72137M are PLL frequency synthesizers for use in radio/cassette players. They allow high-performance AM/FM tuners to be implemented easily.

### Features

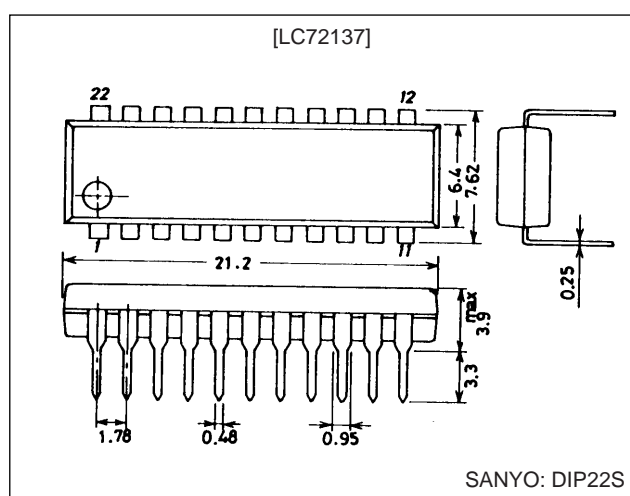
- High-speed programmable frequency divider
  - FMIN: 10 to 160 MHz.....Pulse swallower (divide-by-two prescaler built in)
  - AMIN: 2 to 40 MHz.....Pulse swallower 0.5 to 10 MHz.....Direct division
- IF counter
  - IFIN: 0.4 to 12 MHz.....For use as an AM/FM IF counter
- Reference frequency
  - Selectable from one of eight frequencies (crystal oscillator: 75 kHz)  
1, 3, 5, 3.125, 6.25, 12.5, 15, and 25 kHz
- Phase comparator
  - Supports dead zone control
  - Built-in unlock detection circuit
  - Built-in deadlock clear circuit
- Built-in MOS transistor for forming an active low-pass filter
- I/O ports
  - Dedicated output ports: 4
  - I/O ports: 2
  - Supports clock time base output
- Serial Data I/O
  - Supports CCB format communication with the system controller.
- Operating ranges
  - Supply voltage: 2.5 to 3.6 V
  - Operating temperature: -20 to +70°C
- Packages
  - DIP22S/MFP20

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

### Package Dimensions

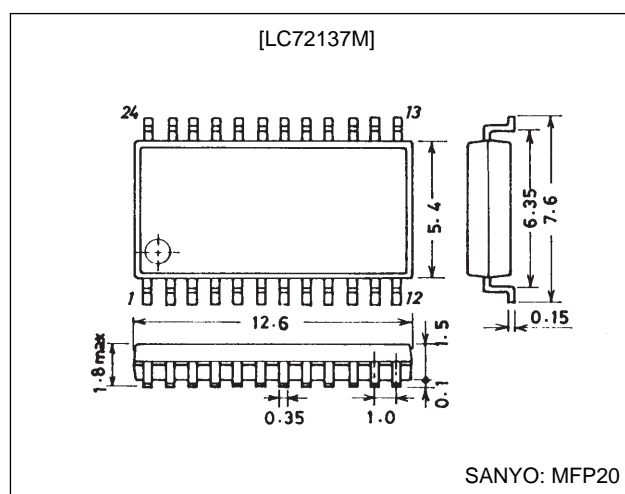
unit: mm

#### 3059-DIP22S



unit: mm

#### 3036B-MFP20



## Specifications

**Absolute Maximum Ratings at Ta = 25°C, V<sub>SS</sub> = 0 V**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD</sub>	−0.3 to +7.0	V
Maximum input voltage	V <sub>IN1</sub> max	CE, CL, DI, AIN	−0.3 to +7.0	V
	V <sub>IN2</sub> max	XIN, FMIN, AMIN, IFIN	−0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>IN3</sub> max	IO1, IO2	−0.3 to +15	V
	V <sub>O1</sub> max	DO	−0.3 to +7.0	V
Maximum output voltage	V <sub>O2</sub> max	XOUT, PD	−0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>O3</sub> max	BO1 to BO5, BOF, IO1, IO2, AOUT	−0.3 to +15	V
Maximum output current	I <sub>O</sub> max	BO1 to BO4, IO1, IO2, DO, AOUT	0 to 6.0	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C: LC72136N (DIP22S)	350	mW
		Ta ≤ 70°C: LC72136NM (MFP20)	180	mW
Operating temperature	Topr		−20 to +70	°C
Storage temperature	Tstg		−40 to +125	°C

**Allowable Operating Ranges at Ta = −20 to +70°C, V<sub>SS</sub> = 0 V**

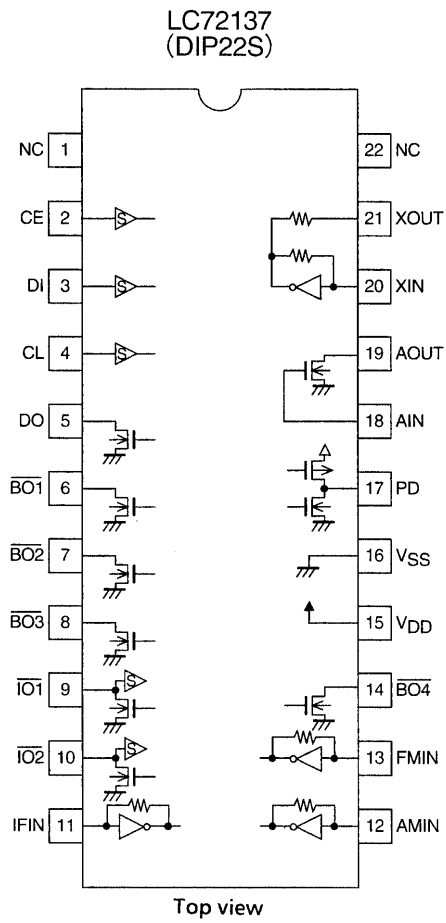
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	2.5		3.6	V
Input high-level voltage	V <sub>IH1</sub>	CE, CL, DI	0.7 V <sub>DD</sub>		6.5	V
	V <sub>IH2</sub>	IO1, IO2	0.7 V <sub>DD</sub>		13	V
Input low-level voltage	V <sub>IL</sub>	CE, CL, DI, IO1, IO2	0		0.3 V <sub>DD</sub>	V
Output voltage	V <sub>O1</sub>	DO	0		6.5	V
	V <sub>O2</sub>	BO1 to BO4, IO1, IO2, AOUT	0		13	V
Input frequency	f <sub>IN1</sub>	XIN: V <sub>IN1</sub>		75		kHz
	f <sub>IN2</sub>	FMIN: V <sub>IN2</sub>	10		160	MHz
	f <sub>IN3</sub>	AMIN: V <sub>IN3</sub> , SNS = 1	2		40	MHz
	f <sub>IN4</sub>	AMIN: V <sub>IN4</sub> , SNS = 0	0.5		10	MHz
	f <sub>IN5</sub>	IFIN: V <sub>IN5</sub>	0.4		12	MHz
Input amplitude	V <sub>IN1</sub>	XIN: f <sub>IN1</sub>	200		800	mVrms
	V <sub>IN2-1</sub>	FMIN: f = 10 to 130 MHz	20		800	mVrms
	V <sub>IN2-2</sub>	FMIN: f = 130 to 160 MHz	40		800	mVrms
	V <sub>IN3</sub>	AMIN: f <sub>IN3</sub> , SNS = 1	40		800	mVrms
	V <sub>IN4</sub>	AMIN: f <sub>IN4</sub> , SNS = 0	40		800	mVrms
	V <sub>IN5-1</sub>	IFIN: f <sub>IN5</sub> , IFS = 1	40		800	mVrms
	V <sub>IN5-2</sub>	IFIN: f <sub>IN6</sub> , IFS = 0	70		800	mVrms
Guaranteed crystal oscillator frequency	Xtal	XIN, XOUT *		75		kHz

\* Note : Recommended crystal oscillator CI value : CI ≤ 35 kΩ

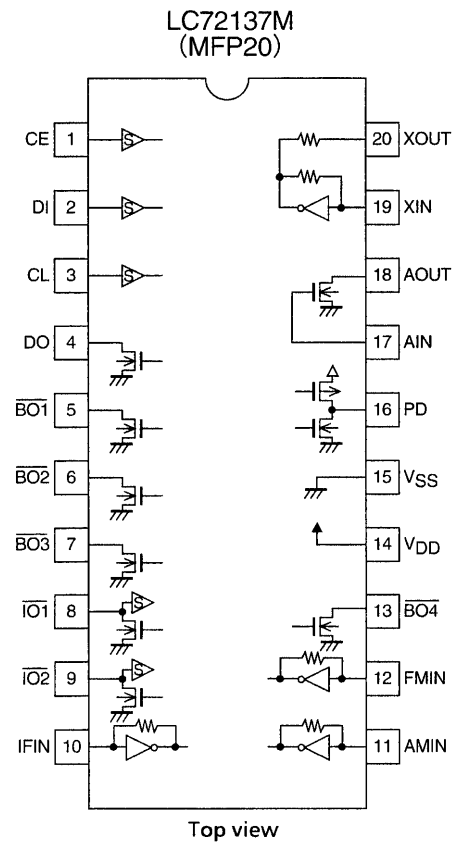
## Electrical Characteristics within the allowable operating ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Internal feedback resistors	Rf1	XIN		8.0		MΩ
	Rf2	FMIN		500		kΩ
	Rf3	AMIN		500		kΩ
	Rf4	IFIN		250		kΩ
Internal pull-down resistors	Rpd1	FMIN		200		kΩ
	Rpd2	AMIN		200		kΩ
Internal output resistor	Rd	XOUT		250		kΩ
Hysteresis	V <sub>HIS</sub>	CE, CL, DI, IO1, IO2		0.1 V <sub>DD</sub>		V
Output high-level voltage	V <sub>OH1</sub>	PD: I <sub>O</sub> = -1 mA	V <sub>DD</sub> - 1.0			V
Output low-level voltage	V <sub>OL1</sub>	PD: I <sub>O</sub> = 1 mA			1.0	V
	V <sub>OL2</sub>	BO1 to BO4, IO1, IO2; I <sub>O</sub> = 1 mA			0.25	V
		BO1 to BO4, IO1, IO2; I <sub>O</sub> = 5 mA			1.25	V
	V <sub>OL3</sub>	DO: I <sub>O</sub> = 1 mA			0.25	V
	V <sub>OL4</sub>	AOUT, A <sub>IN</sub> = 1.3 V			0.5	
Input high-level voltage	I <sub>IH1</sub>	CE, CL, DI: V <sub>I</sub> = 6.5 V			5.0	μA
	I <sub>IH2</sub>	IO1, IO2: V <sub>I</sub> = 13 V			5.0	μA
	I <sub>IH3</sub>	XIN: V <sub>I</sub> = V <sub>DD</sub>	0.16		0.9	μA
	I <sub>IH4</sub>	FMIN, AMIN: V <sub>I</sub> = V <sub>DD</sub>	2.5		15	μA
	I <sub>IH5</sub>	IFIN: V <sub>I</sub> = V <sub>DD</sub>	5.0		30	μA
	I <sub>IH6</sub>	AIN: V <sub>I</sub> = 6.5 V			200	nA
Input low-level current	I <sub>IL1</sub>	CE, CL, DI: V <sub>I</sub> = 0 V			5.0	μA
	I <sub>IL2</sub>	IO1, IO2: V <sub>I</sub> = 0 V			5.0	μA
	I <sub>IL3</sub>	XIN: V <sub>I</sub> = 0 V	0.16		0.9	μA
	I <sub>IL4</sub>	FMIN, AMIN: V <sub>I</sub> = 0 V	2.5		15	μA
	I <sub>IL5</sub>	IFIN: V <sub>I</sub> = 0 V	5.0		30	μA
	I <sub>IL6</sub>	AIN: V <sub>I</sub> = 0 V			200	nA
Output off leakage current	I <sub>OFF1</sub>	BO1 to BO4, AOUT, IO1, IO2: V <sub>O</sub> = 13 V			5.0	μA
	I <sub>OFF2</sub>	DO: V <sub>O</sub> = 6.5 V			5.0	μA
High-level three-state off leakage current	I <sub>OFFH</sub>	PD: V <sub>O</sub> = V <sub>DD</sub>		0.01	200	nA
Low-level three-state off leakage current	I <sub>OFFL</sub>	PD: V <sub>O</sub> = 0 V		0.01	200	nA
Input capacitance	C <sub>IN</sub>	FMIN		6		pF
Current drain	I <sub>DD1</sub>	V <sub>DD</sub> : Xtal = 75 kHz, f <sub>IN2</sub> = 130 MHz, V <sub>IN2</sub> = 20 mVrms		2.5	6	mA
	I <sub>DD2</sub>	V <sub>DD</sub> : PLL block stopped (PLL inhibit), Xtal oscillator operating (Xtal = 75 kHz)		20		mA
	I <sub>DD3</sub>	V <sub>DD</sub> : PLL block stopped, Xtal oscillator stopped			10	μA

## Pin Assignments

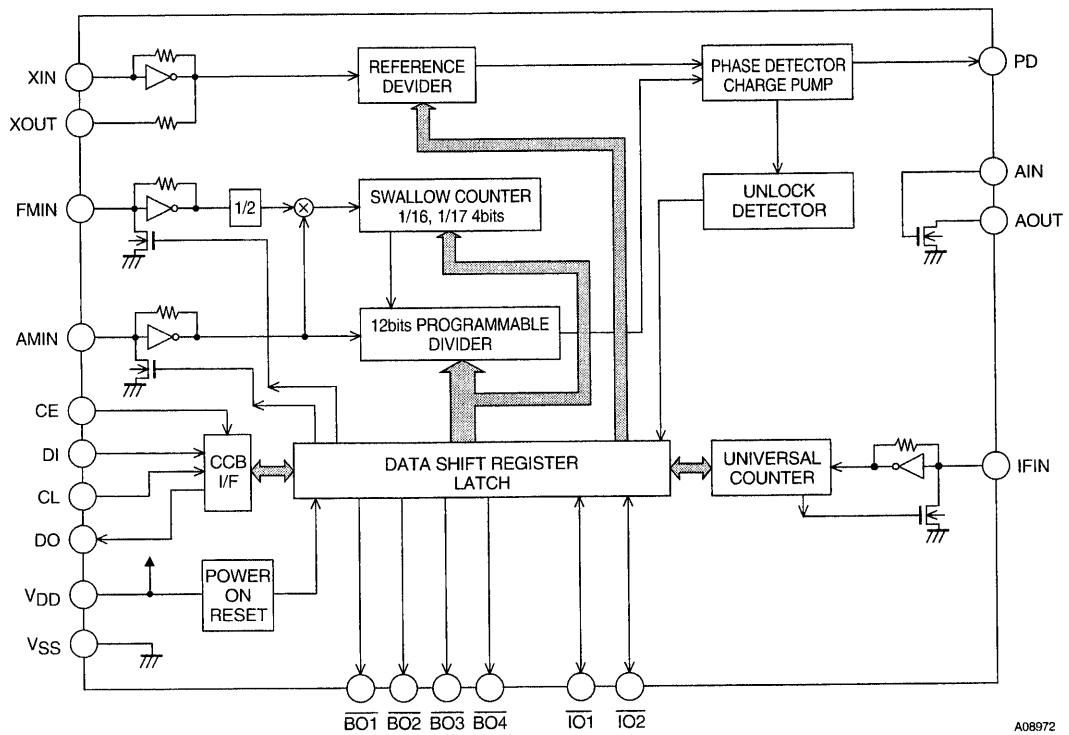


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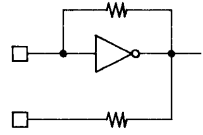
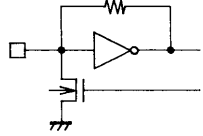
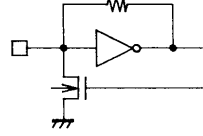
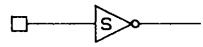
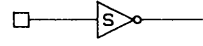
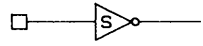
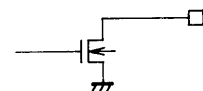
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# Block Diagram



# LC72137, 72137M

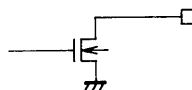
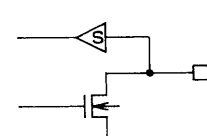
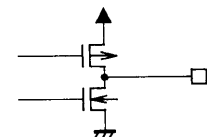
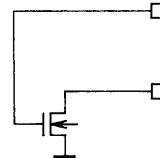
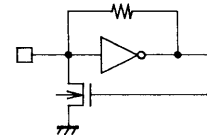
## Pin Descriptions

Symbol	Pin No. (MFP pin numbers are in parentheses.)	Type	Functions	Circuit configuration
XIN XOUT	20 (19) 21 (21)	Xtal	<ul style="list-style-type: none"> <li>Crystal oscillator connections (75 kHz)</li> </ul>	 A03414
FMIN	13 (12)	Local oscillator signal input	<ul style="list-style-type: none"> <li>FMIN is selected when the serial data input DVS bit is set to 1.</li> <li>The input frequency range is from 10 to 160 MHz.</li> <li>The input signal passes through the internal divide-by-two prescaler and is input to the swallow counter.</li> <li>The divisor can be in the range 272 to 65535. However, since the signal has passed through the divide-by-two prescaler, the actual divisor is twice the set value.</li> </ul>	 A02599
AMIN	12 (11)	Local oscillator signal input	<ul style="list-style-type: none"> <li>AMIN is selected when the serial data input DVS bit is set to 0.</li> <li>When the serial data input SNS bit is set to 1:               <ul style="list-style-type: none"> <li>The input frequency range is 2 to 40 MHz.</li> <li>The signal is directly input to the swallow counter.</li> <li>The divisor can be in the range 272 to 65535, and the divisor used will be the value set.</li> </ul> </li> <li>When the serial data input SNS bit is set to 0:               <ul style="list-style-type: none"> <li>The input frequency range is 0.5 to 10 MHz.</li> <li>The signal is directly input to a 12-bit programmable divider.</li> <li>The divisor can be in the range 4 to 4095, and the divisor used will be the value set.</li> </ul> </li> </ul>	 A02599
CE	2 (1)	Chip enable	<ul style="list-style-type: none"> <li>Set this pin high when inputting (DI) or outputting (DO) serial data.</li> </ul>	 A02600
DI	3 (2)	Input data	<ul style="list-style-type: none"> <li>Inputs serial data transferred from the controller to the LC72137.</li> </ul>	 A02600
CL	4 (3)	Clock	<ul style="list-style-type: none"> <li>Used as the synchronization clock when inputting (DI) or outputting (DO) serial data.</li> </ul>	 A02600
DO	5 (4)	Output data	<ul style="list-style-type: none"> <li>Outputs serial data transferred from the LC72137 to the controller. The data output is determined by the DOC0 to DOC2 bits in the serial data.</li> </ul>	 A02601
V <sub>DD</sub>	15 (14)	Power supply	<ul style="list-style-type: none"> <li>The LC72137 power supply pin. (V<sub>DD</sub> = 2.5 to 3.6 V)</li> <li>The power on reset circuit operates when power is first applied.</li> </ul>	
V <sub>SS</sub>	16 (15)	Ground	<ul style="list-style-type: none"> <li>The LC72137N ground</li> </ul>	

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# LC72137, 72137M

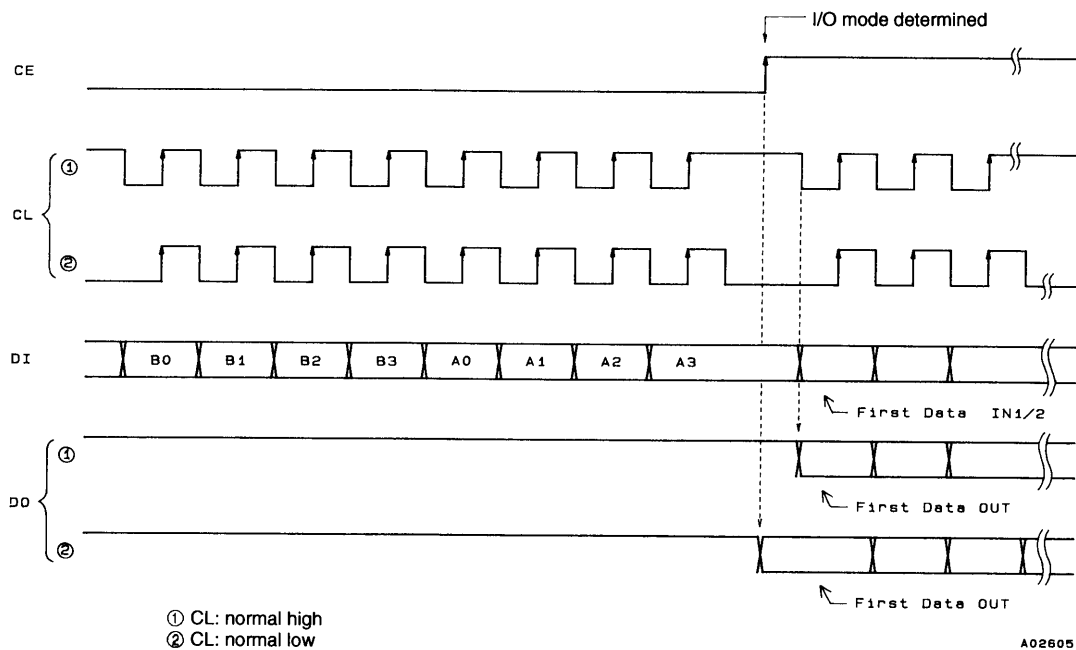
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Symbol	Pin No. (MFP pin numbers are in parentheses.)	Type	Functions	Circuit configuration
$\overline{\text{BO1}}$ $\overline{\text{BO2}}$ $\overline{\text{BO3}}$ $\overline{\text{BO4}}$	6 (5) 7 (6) 8 (7) 14 (13)	Output ports	<ul style="list-style-type: none"> <li>Dedicated outputs</li> <li>The output states are determined by the BO1 to BO5 bits in the serial data. Data: 0 = open, 1 = low</li> <li>A time base signal (8 Hz) can be output from the <math>\overline{\text{BO1}}</math> pin. (When the serial data TBC bit is set to 1.)</li> </ul>	 A02501
$\overline{\text{IO1}}$ $\overline{\text{IO2}}$	9 (8) 10 (9)	Input or output ports	<ul style="list-style-type: none"> <li>I/O dual-use pins</li> <li>The direction (input or output) is determined by bits IOC1 and IOC2 in the serial data. Data: 0 = input port, 1 = output port</li> <li>When specified for use as input ports: The state of the input pin is transmitted to the controller over the DO pin. Input state: low = 0 data value                   high = 1 data value</li> <li>When specified for use as output ports: The output states are determined by the IO1 and IO2 bits in the serial data. Data: 0 = open, 1 = low</li> <li>These pins function as input pins following a power on reset.</li> </ul>	 A02502
PD	17 (16)	Charge pump output	<ul style="list-style-type: none"> <li>PLL charge pump output When the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, a high level is output from the PD pin. Similarly, when that frequency is lower, a low level is output. The PD pin goes to the high-impedance state when the frequencies match.</li> </ul>	 A02503
AIN AOUT	18 (17) 19 (18)	LPF amplifier transistor connections	<ul style="list-style-type: none"> <li>The n-channel MOS transistor used for the PLL active low-pass filter.</li> </ul>	 A02504
IFIN	10 (9)	IF counter	<ul style="list-style-type: none"> <li>Accepts an input in the frequency range 0.4 to 12 MHz.</li> <li>The input signal is directly transmitted to the IF counter.</li> <li>The result is output starting the MSB of the IF counter using the DO pin.</li> <li>Four measurement periods are supported: 4, 8, 16, and 32 ms.</li> </ul>	 A02599
NC	1 (-) 22 (-)	NC Pin	<ul style="list-style-type: none"> <li>No connection</li> </ul>	

## Serial Data I/O Procedures

The LC72137 inputs and outputs data using the Sanyo CCB (computer control bus) audio IC serial bus format. This IC adopts an 8-bit address format CCB.

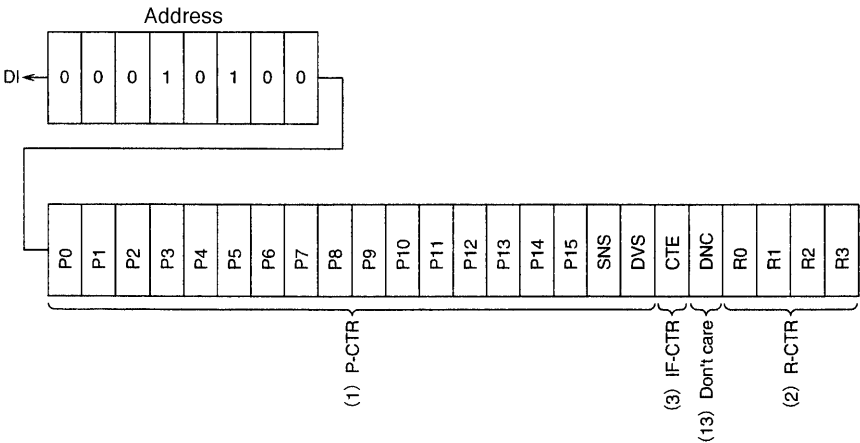
	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
1	IN1 (82)	0	0	0	1	0	1	0	0	<ul style="list-style-type: none"> <li>Control data input mode (serial data input)</li> <li>24 data bits are input.</li> <li>See the "DI Control Data (serial data input) Structure" item for details on the meaning of the input data.</li> </ul>
2	IN2 (92)	1	0	0	1	0	1	0	0	<ul style="list-style-type: none"> <li>Control data input mode (serial data input)</li> <li>24 data bits are input.</li> <li>See the "DI Control Data (serial data input) Structure" item for details on the meaning of the input data.</li> </ul>
3	OUT (A2)	0	1	0	1	0	1	0	0	<ul style="list-style-type: none"> <li>Data output mode (serial data output)</li> <li>The number of bits output is equal to the number of clock cycles.</li> <li>See the "DO Output Data (Serial Data Output) Structure" item for details on the meaning of the output data.</li> </ul>





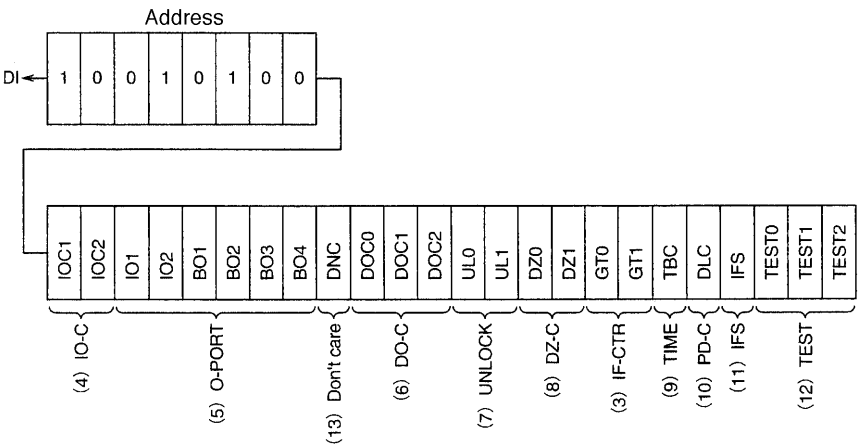
DI Control Data (serial data input) Structure

1. IN1 Mode



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2. IN2 Mode



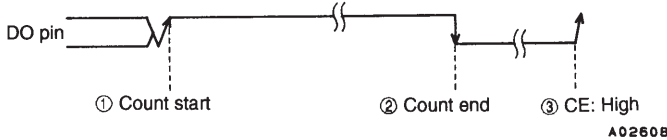
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## DI Control Data Descriptions

No.	Control block/data	Description	Related data																																																																																					
(1)	Programmable divider data P0 to P15  DVS, SNS	<ul style="list-style-type: none"><li>Data that sets the programmable divider A binary value in which P15 is the MSB. The LSB changes depending on DVS and SNS. (*: Don't care.)</li></ul> <table><tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th><th>Actual divisor</th></tr><tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the value of the setting</td></tr><tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The value of the setting</td></tr><tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The value of the setting</td></tr></table> <p>Note: P0 to P3 are ignored when P4 is the LSB.</p> <ul style="list-style-type: none"><li>Selects the signal input pin (AMIN or FMIN) for the programmable divider, switches the frequency range. (*: Don't care.)</li></ul> <table><tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input frequency range</th></tr><tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160 MHz</td></tr><tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr><tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr></table> <p>Note: See the "Programmable Divider" item for details.</p>	DVS	SNS	LSB	Divisor setting (N)	Actual divisor	1	*	P0	272 to 65535	Twice the value of the setting	0	1	P0	272 to 65535	The value of the setting	0	0	P4	4 to 4095	The value of the setting	DVS	SNS	Input pin	Input frequency range	1	*	FMIN	10 to 160 MHz	0	1	AMIN	2 to 40 MHz	0	0	AMIN	0.5 to 10 MHz																																																		
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0	1	AMIN	2 to 40 MHz																																																																																					
0	0	AMIN	0.5 to 10 MHz																																																																																					
(2)	Reference divider data R0 to R3	<ul style="list-style-type: none"><li>Reference frequency (fref) selection data</li></ul> <table><tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency (kHz)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + Xtal OSC STOP</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr></table> <p>Note: PLL INHIBIT The programmable divider and IF counter blocks are stopped, the FMIN, AMIN, and IFIN pins go to the pulled-down state, and the charge pump output pin goes to the high-impedance state.</p>	R3	R2	R1	R0	Reference frequency (kHz)	0	0	0	0	25	0	0	0	1	25	0	0	1	0	25	0	0	1	1	25	0	1	0	0	12.5	0	1	0	1	6.25	0	1	1	0	3.125	0	1	1	1	3.125	1	0	0	0	5	1	0	0	1	5	1	0	1	0	5	1	0	1	1	1	1	1	0	0	3	1	1	0	1	15	1	1	1	0	PLL INHIBIT + Xtal OSC STOP	1	1	1	1	PLL INHIBIT	
R3	R2	R1	R0	Reference frequency (kHz)																																																																																				
0	0	0	0	25																																																																																				
0	0	0	1	25																																																																																				
0	0	1	0	25																																																																																				
0	0	1	1	25																																																																																				
0	1	0	0	12.5																																																																																				
0	1	0	1	6.25																																																																																				
0	1	1	0	3.125																																																																																				
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1	1	0	1	15																																																																																				
1	1	1	0	PLL INHIBIT + Xtal OSC STOP																																																																																				
1	1	1	1	PLL INHIBIT																																																																																				
(3)	IF counter control data CTE  GT0, GT1	<ul style="list-style-type: none"><li>IF counter measurement start specification CTE = 1: Counter start CTE = 0: Counter reset</li><li>IF counter measurement time determination</li></ul> <table><tr><th>GT1</th><th>GT0</th><th>Measurement time (ms)</th><th>Wait time (ms)</th></tr><tr><td>0</td><td>0</td><td>4</td><td>3 to 4</td></tr><tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr><tr><td>1</td><td>0</td><td>16</td><td>7 to 8</td></tr><tr><td>1</td><td>1</td><td>32</td><td>7 to 8</td></tr></table> <p>Note: See the "IF Counter Structure" item for details.</p>	GT1	GT0	Measurement time (ms)	Wait time (ms)	0	0	4	3 to 4	0	1	8	3 to 4	1	0	16	7 to 8	1	1	32	7 to 8	IFS																																																																	
GT1	GT0	Measurement time (ms)	Wait time (ms)																																																																																					
0	0	4	3 to 4																																																																																					
0	1	8	3 to 4																																																																																					
1	0	16	7 to 8																																																																																					
1	1	32	7 to 8																																																																																					
(4)	I/O port specification data IOC1, IOC2	<ul style="list-style-type: none"><li>Data that specifies input or output for the I/O dual-use pins (<math>\overline{IO1}</math>, <math>\overline{IO2}</math>) Data: 0 = input mode, 1 = output mode</li></ul>																																																																																						
(5)	Output port data BO1 to BO4, IO1, IO2	<ul style="list-style-type: none"><li><math>\overline{BO1}</math> to <math>\overline{BO4}</math>, <math>\overline{IO1}</math>, and <math>\overline{IO2}</math> output state data Data: 0 = open, 1 = low</li><li>"Data = 0: Open" is selected following a power-on reset.</li></ul>	IOC1 IOC2																																																																																					

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Continued from preceding page.

No.	Control block/data	Description	Related data																																				
(6)	DO pin control data DOC0, DOC1, DOC2	<div>• Data that determines DO pin output</div> <table><tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Low when the unlock state is detected</td></tr><tr><td>0</td><td>1</td><td>0</td><td>end-UC*<sup>1</sup></td></tr><tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>1</td><td>The <math>\overline{\text{IO1}}</math> pin state*<sup>2</sup></td></tr><tr><td>1</td><td>1</td><td>0</td><td>The <math>\overline{\text{IO2}}</math> pin state*<sup>2</sup></td></tr><tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr></table> <p>The open state is selected following a power-on reset.</p> <p>Note: 1. end-UC: IF counter measurement completion check</p> <div></div> <p>① When end-UC is set and an IF count is started (CTE = 0 → 1), the DO pin automatically goes to the open state.</p> <p>② When the IF count measurement completes, the DO pin goes low and the count completion check operation is enabled.</p> <p>③ The DO pin goes to the open state due to serial data I/O (CE: high).</p> <p>2. Goes to the open state if the IO pin itself is set to be an output port.</p> <p>Caution: The DO pin always goes to the open state during the data input period (during the period when CE is high in mode IN1 or IN2), regardless of the values of the DO pin control data (DOC0 to DOC2). Also, the DO pin outputs the content of the internal DO serial data in synchronization with the CL pin signal during the data output period (during the period when CE is high in the OUT mode) regardless of the values of the DO pin control data (DOC0 to DOC2).</p>	DOC2	DOC1	DOC0	DO pin state	0	0	0	Open	0	0	1	Low when the unlock state is detected	0	1	0	end-UC* <sup>1</sup>	0	1	1	Open	1	0	0	Open	1	0	1	The $\overline{\text{IO1}}$ pin state* <sup>2</sup>	1	1	0	The $\overline{\text{IO2}}$ pin state* <sup>2</sup>	1	1	1	Open	UL0, UL1, CTE, IOC1, IOC2
DOC2	DOC1	DOC0	DO pin state																																				
0	0	0	Open																																				
0	0	1	Low when the unlock state is detected																																				
0	1	0	end-UC* <sup>1</sup>																																				
0	1	1	Open																																				
1	0	0	Open																																				
1	0	1	The $\overline{\text{IO1}}$ pin state* <sup>2</sup>																																				
1	1	0	The $\overline{\text{IO2}}$ pin state* <sup>2</sup>																																				
1	1	1	Open																																				
(7)	Unlock detection data UL0, UL1	<div>• Selects the phase error (ϕE) detection range for PLL lock discrimination.</div> <p>When a phase error greater than the specified range occurs, the LC72136N determines that the PLL is unlocked. (*: Don't care.)</p> <table><tr><th>UL1</th><th>UL0</th><th>ϕE detection width</th><th>Detector output</th></tr><tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>ϕE is output directly</td></tr><tr><td>1</td><td>*</td><td>±6.67 μs</td><td>ϕE is extended by 1 to 2 ms</td></tr></table> <p>Note: When unlocked, the DO pin goes low and the serial data output UL bit is 0.</p>	UL1	UL0	ϕE detection width	Detector output	0	0	Stopped	Open	0	1	0	ϕE is output directly	1	*	±6.67 μs	ϕE is extended by 1 to 2 ms	DOC0, DOC1, DOC2																				
UL1	UL0	ϕE detection width	Detector output																																				
0	0	Stopped	Open																																				
0	1	0	ϕE is output directly																																				
1	*	±6.67 μs	ϕE is extended by 1 to 2 ms																																				
(8)	Phase comparator control data DZ0, DZ1	<div>• Phase comparator dead zone control data</div> <table><tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr><tr><td>0</td><td>0</td><td>DZA</td></tr><tr><td>0</td><td>1</td><td>DZB</td></tr><tr><td>1</td><td>0</td><td>DZC</td></tr><tr><td>1</td><td>1</td><td>DZD</td></tr></table> <p>Dead zone width: DZA &lt; DZB &lt; DZC &lt; DZD</p>	DZ1	DZ0	Dead zone mode	0	0	DZA	0	1	DZB	1	0	DZC	1	1	DZD																						
DZ1	DZ0	Dead zone mode																																					
0	0	DZA																																					
0	1	DZB																																					
1	0	DZC																																					
1	1	DZD																																					
(9)	Clock time base TBC	<div>• An 8 Hz 40% duty clock time base signal can be output from <math>\overline{\text{BO1}}</math> by setting TBC to 1.</div> <p>(The BO1 data will be ignored.)</p>	BO1																																				
(10)	Charge pump control data DLC	<div>• Data that forcibly controls the charge pump output</div> <table><tr><th>DLC</th><th>Charge pump output</th></tr><tr><td>0</td><td>Normal operation</td></tr><tr><td>1</td><td>Forced low</td></tr></table> <p>Note: The LC72137 provides a technique for escaping from deadlock by setting Vtune to VCC (deadlock clear circuit). This is used when the circuit is deadlocked due to the VCO oscillator being stopped by the VCO control voltage (Vtune) being 0 V.</p>	DLC	Charge pump output	0	Normal operation	1	Forced low																															
DLC	Charge pump output																																						
0	Normal operation																																						
1	Forced low																																						

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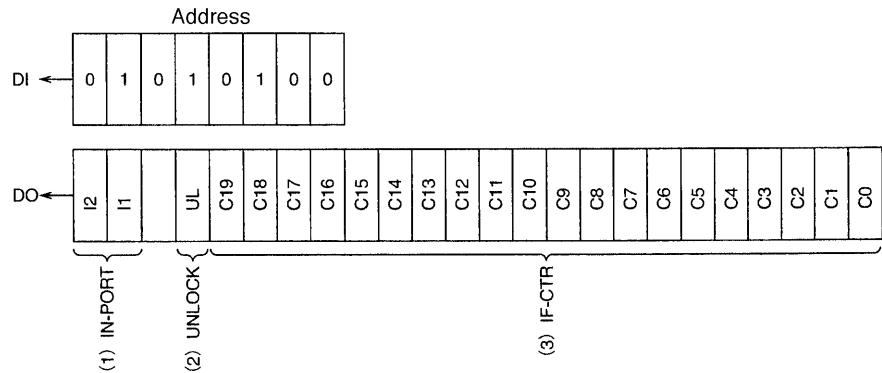
## LC72137, 72137M

Continued from preceding page.

No.	Control block/data	Description	Related data
(11)	IF counter control data IFS	<ul style="list-style-type: none"> <li>This data should be set to 1 in normal operation. Setting this data to 0 switches the LC72137 to a reduced input sensitivity mode in which the sensitivity is reduced by 10 to 30 mVrms.</li> </ul>	
(12)	LSI test data TEST 0 to TEST2	<ul style="list-style-type: none"> <li>IC test data  <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> TEST0 TEST1 TEST2 </div> <div style="border-left: 1px solid black; padding-left: 5px;"> All three bits must be set to 0. </div> </div> </li> <li>All the test data is set to 0 at a power-on reset.</li> </ul>	
(13)	DNC	Data is set to 0	

### DO Output Data (Serial Data Output) Structure

#### 3. OUT mode



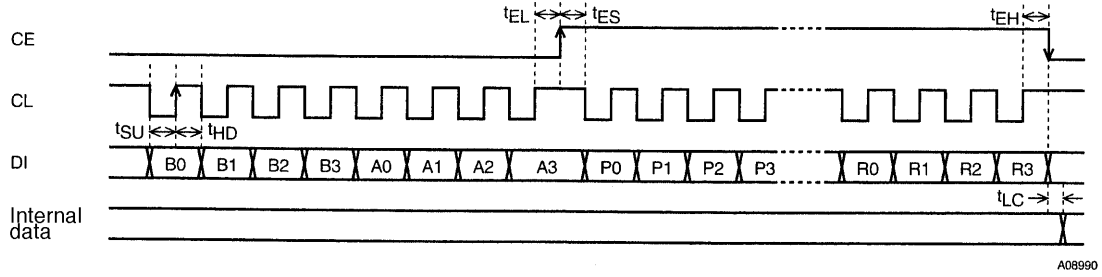
A08989

### DO Output Data

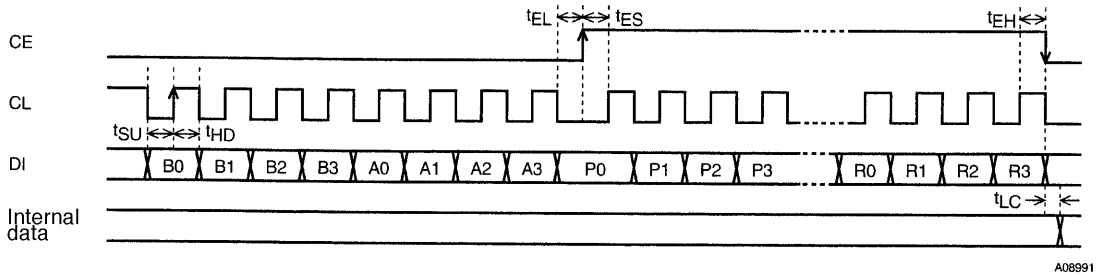
No.	Control block/data	Description	Related data
(1)	I/O port data I2, I1	<ul style="list-style-type: none"> <li>Data latched from the states of the I/O ports, pins <math>\overline{IO1}</math> and <math>\overline{IO2}</math>.</li> <li>This data reflects the pin states, regardless of whether they are in input or output mode.</li> <li>The data is latched when OUT mode is selected.</li> </ul> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> I1 ← <math>\overline{IO1}</math> pin state I2 ← <math>\overline{IO2}</math> pin state </div> <div style="border-left: 1px solid black; padding-left: 5px;"> High: 1 Low: 0 </div> </div>	IOC1, IOC2
(2)	PLL unlock data UL	<ul style="list-style-type: none"> <li>Data latched from the state of the unlock detection circuit</li> <li>UL ← 0: Unlocked</li> <li>UL ← 1: Locked or in detection stopped mode</li> </ul>	UL0, UL1
(3)	IF counter binary data C19 to C0	<ul style="list-style-type: none"> <li>Data latched from the state of the IF counter, which is a 20-bit binary counter.</li> <li>C19 ← Binary counter MSB</li> <li>C0 ← Binary counter LSB</li> </ul>	CTE, GT0, GT1

**Serial Data Input (IN1/IN2)  $t_{SU}$ ,  $t_{HD}$ ,  $t_{EL}$ ,  $t_{ES}$ ,  $t_{EH}$ ,  $\geq 0.75 \mu s$ ,  $t_{LC} < 0.75 \mu s$**

1. CL: Normal high

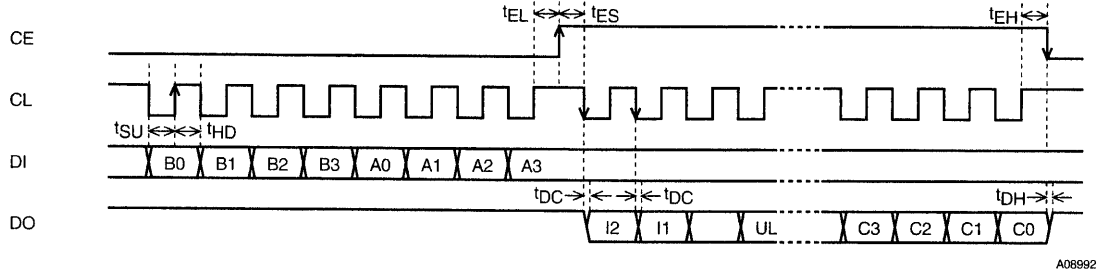


2. CL: Normal low

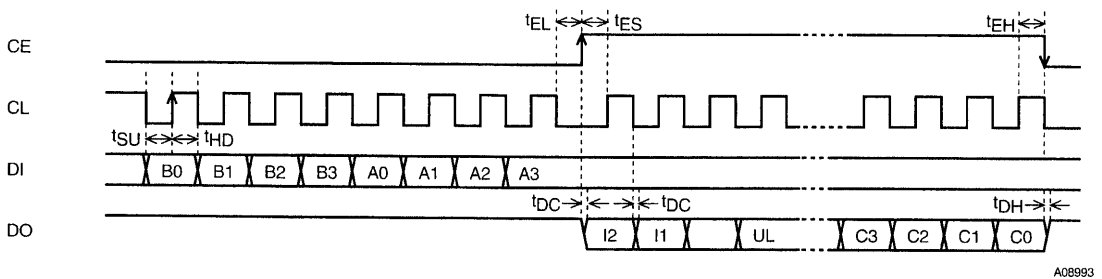


**Serial Data Output (OUT)  $t_{SU}$ ,  $t_{HD}$ ,  $t_{EL}$ ,  $t_{ES}$ ,  $t_{EH}$ ,  $\geq 0.75 \mu s$ ,  $t_{DC}$ ,  $t_{DH} < 0.35 \mu s$**

1. CL: Normal high

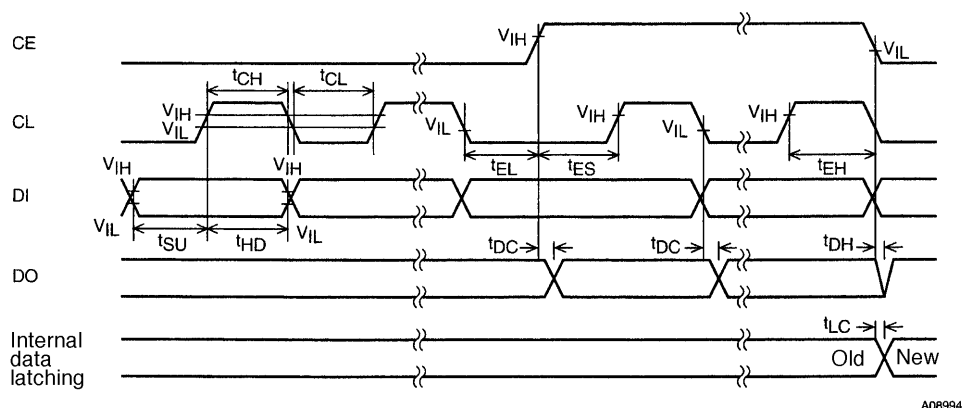


2. CL: Normal low



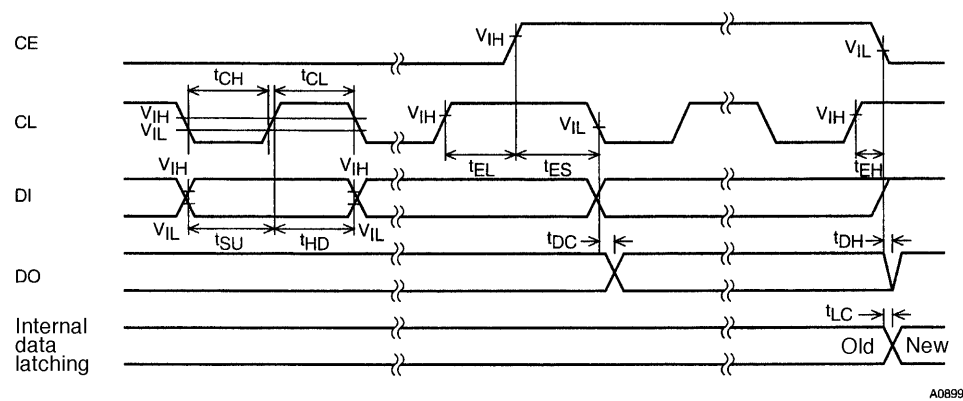
Note: Since the DO pin is an n-channel open drain circuit, the times for the data to change ( $t_{DC}$  and  $t_{DH}$ ) will differ depending on the value of the pull-up resistor, printed circuit board capacitance.

## Serial Data Timing



A08994

### CL Stopped at the Low Level



A08995

### CL Stopped at the High Level

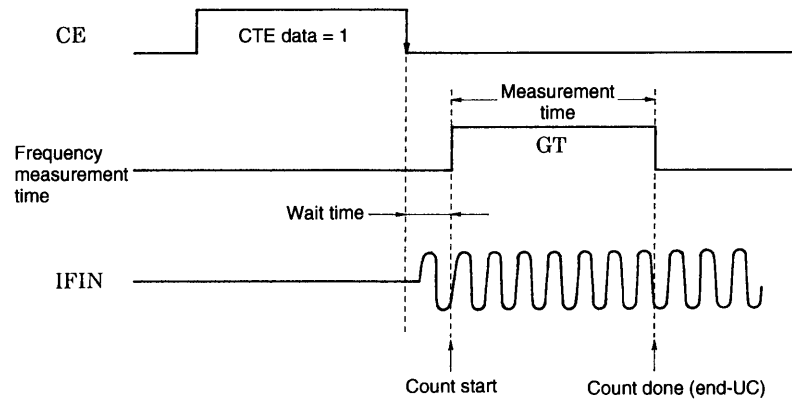
Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Data setup time	$t_{SU}$	DI, CL		0.75			$\mu s$
Data hold time	$t_{HD}$	DI, CL		0.75			$\mu s$
Clock low-level time	$t_{CL}$	CL		0.75			$\mu s$
Clock high-level time	$t_{CH}$	CL		0.75			$\mu s$
CE wait time	$t_{EL}$	CE, CL		0.75			$\mu s$
CE setup time	$t_{ES}$	CE, CL		0.75			$\mu s$
CE hold time	$t_{EH}$	CE, CL		0.75			$\mu s$
Data latch change time	$t_{LC}$					0.75	$\mu s$
Data output time	$t_{DC}$	DO, CL	These times depend on the pull-up resistance and the printed circuit board capacitances.			0.35	$\mu s$
	$t_{DH}$	DO, CE				0.35	$\mu s$







## IF Counter Operation



A02623

Before starting the IF count, the IF counter must be reset in advance by setting CTE in the serial data to 0. The IF count is started by changing the CTE bit in the serial data from 0 to 1. The serial data is latched by the LC72137 when the CE pin is dropped from high to low. The IF signal must be supplied to the IFIN pin in the period between the point the CE pin goes low and the end of the wait time at the latest. Next, the value of the IF count at the end of the measurement period must be read out during the period CTE is 1. This is because the IF counter is reset when CTE is set to 0.

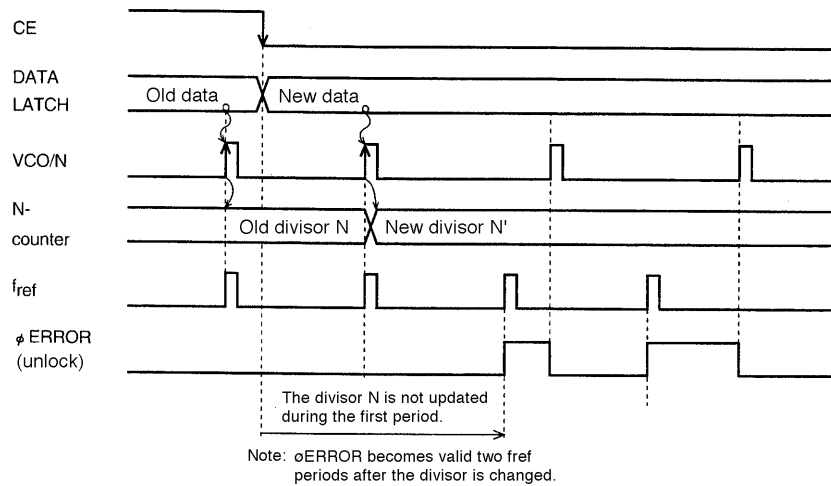
**Note:** When operating the IF counter, the control microcontroller must first check the state of the IF-IC SD (station detect) signal and only after determining that the SD signal is present turn on IF buffer output and execute an IF count operation. Auto-search techniques that use only the IF counter are not recommended, since it is possible for IF buffer leakage output to cause incorrect stops at points where there is no station.

If the auto-search technique is implemented using only the IF counter in combination with an IF-IC without SD output, sensitivity-degradation mode (IFS = 0) should be selected.

## Unlock Detection Timing

### 1. Unlock Detection Determination Timing

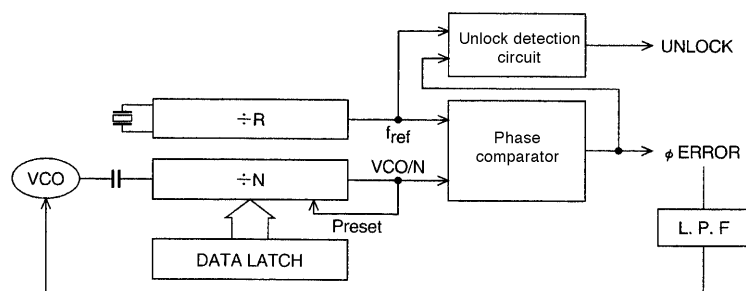
Unlock detection is performed in the reference frequency ( $f_{ref}$ ) period (interval). Therefore, in principle, unlock determination requires a time longer than the period of the reference frequency. However, immediately after changing the divisor  $N$  (frequency) unlock detection must be performed after waiting at least two periods of the reference frequency.



A09004

**Figure 1 Unlock Detection Timing**

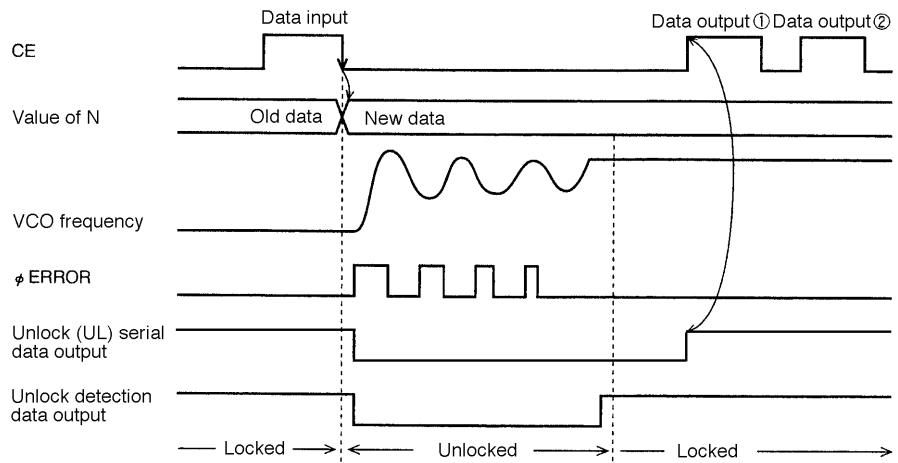
For example, if  $f_{ref}$  is 1 kHz (and thus the period is 1 ms), after changing the divisor  $N$ , the system must wait at least 2 ms before checking for the unlocked state.



A09005

**Figure 2 Circuit Structure**

## 2. Unlock Detection Software

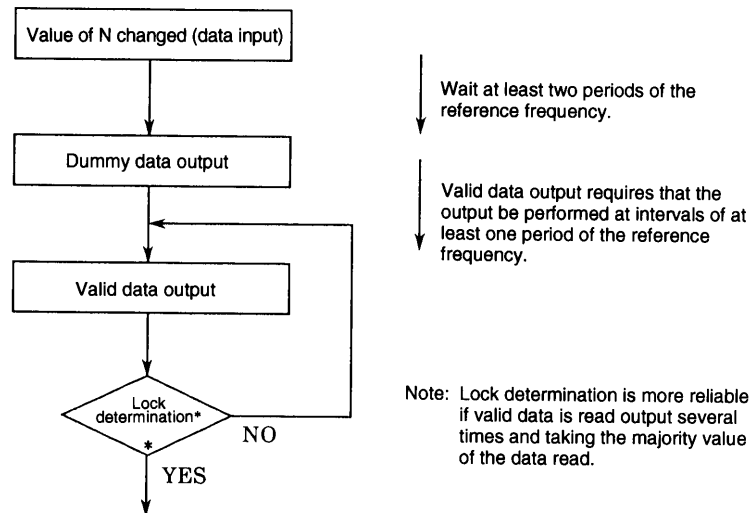


A09006

**Figure 3**

### 3. When Outputting Unlock Data Using Serial Data Output:

Once the LC72137 detects an unlocked state, it does not reset the unlock data (UL) until the next data output (or data input) operation is performed. At the data output ① point in Figure 3, although the VCO frequency is stable (locked), the unlock data remains set to the unlocked state since no data output has been performed since the value of N was changed. Thus, even though the frequency became stable (locked), from the point of view of the data, the circuit is in the unlocked state. Therefore, the data output ① immediately following a change to the value of N should be seen as a dummy data, and the data from the second data output (data output ②) and later outputs should be seen as valid data.



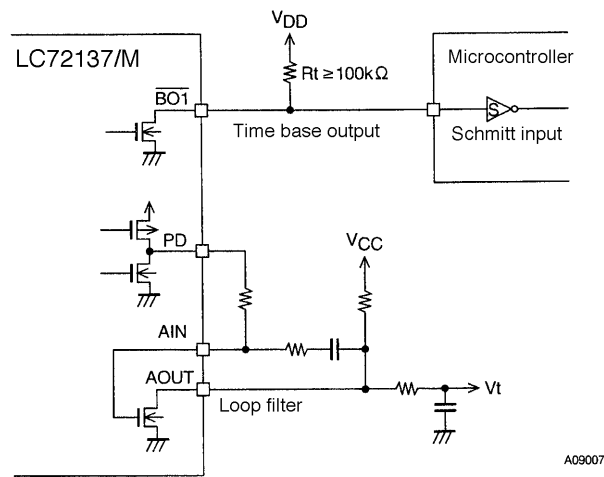
**Lock Determination Flowchart**

### When directly outputting data from the DO pin (set up by the DO pin control data)

Since the DO pin outputs the unlocked state (locked: high, unlocked: low) the timing considerations in the technique described in the previous section are not necessary. After changing the value of N, the locked state can be determined after waiting at least two periods of the reference frequency.

### Notes on Clock Time Base Usage

When the clock time base output is used, the value of the pull-up resistor for the output pin ( $\overline{BO1}$ ) must be at least 100 k $\Omega$ . We recommend the use of a Schmitt input on the receiving controller (microprocessor) to prevent chattering. This is to avoid degradation of the VCO C/N characteristics when using the built-in low-pass filter transistor to form the loop filter. Since the clock time base output pin and the low-pass filter transistor ground are the same mode in the IC, the time base output pin current fluctuations must be suppressed to limit the influence on the low-pass filter.



### Other Items

#### 1. Notes on the Phase Comparator Dead Zone

DZ1	DZ0	Dead-zone mode	Charge pump	Dead zone
0	0	DZA	ON/ON	- -0 s
0	1	DZB	ON/ON	-0 s
1	0	DZC	OFF/OFF	+0 s
1	1	DZD	OFF/OFF	+ +0 s

Since correction pulses are output from the charge pump even if the PLL is locked when the charge pump is in the ON/ON state, the loop can easily become unstable. This point requires special care when designing application circuits.

The following problems may occur in the ON/ON state.

- Side band generation due to reference frequency leakage
- Side band generation due to both the correction pulse envelope and low frequency leakage

Schemes in which a dead zone is present (OFF/OFF) have good loop stability, but have the problem that acquiring a high C/N ratio can be difficult. On the other hand, although it is easy to acquire a high C/N ratio with schemes in which there is no dead zone, it is difficult to achieve high loop stability. Therefore, it can be effective to select DZA or DZB, which have no dead zone, in applications which require an FM S/N ratio in excess of 90 to 100 dB, or in which an increased AM stereo pilot margin is desired. On the other hand, we recommend selecting DZC or DZD, which provide a dead zone, for applications which do not require such a high FM signal-to-noise ratio and in which either AM stereo is not used or an adequate AM stereo pilot margin can be achieved.

#### Dead Zone

The phase comparator compares  $f_p$  to a reference frequency ( $f_r$ ) as shown in Figure 4. Although the characteristics of this circuit (see Figure 5) are such that the output voltage is proportional to the phase difference  $\phi$  (line A), a region (the dead zone) in which it is not possible to compare small phase differences occurs in actual ICs due to internal circuit delays and other factors (line B). A dead zone as small as possible is desirable for products that must provide a high S/N ratio.

However, since a larger dead zone makes this circuit easier to use, a larger dead zone is appropriate for popularly-priced products. This is because it is possible for RF signals to leak from the mixer to the VCO and modulate the VCO in popularly-priced products in the presence of strong RF inputs. When the dead zone is narrow, the circuit outputs correction pulses and this output can further modulate the VCO and generate beat frequencies with the RF signal.

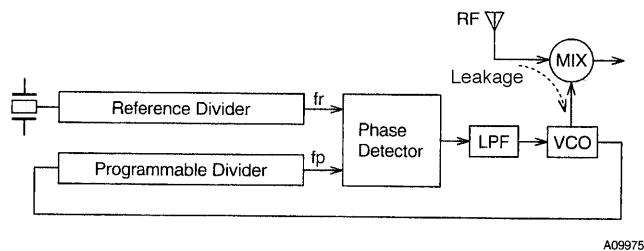


Figure 4

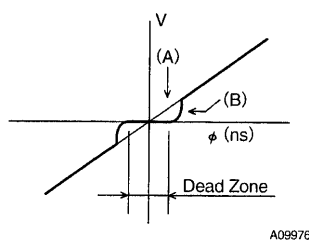


Figure 5

#### 2. Notes on the FMIN, AMIN, and IFIN Pins

Coupling capacitors must be placed as close as possible to their respective pin. A capacitance of about 100 pF is desirable. In particular, if a capacitance of 1000 pF or over is used for the IF pin, the time to reach the bias level will increase and incorrect counting may occur due to the relationship with the wait time.

#### 3. Notes on IF Counting → SD must be used in conjunction with the IF counting time

When using IF counting, always implement IF counting by having the microprocessor determine the presence of the IF-IC SD (station detect) signal and turn on the IF counter buffer only if the SD signal is present. Schemes in which auto-searches are performed with only IF counting are not recommended, since they can stop at points where there is no signal due to leakage output from the IF counter buffer.

4. DO Pin Usage Techniques

In addition to data output mode times, the DO pin can also be used to check for IF counter count completion and for unlock detection output. Also, an input pin state can be output unchanged through the DO pin and input to the controller.

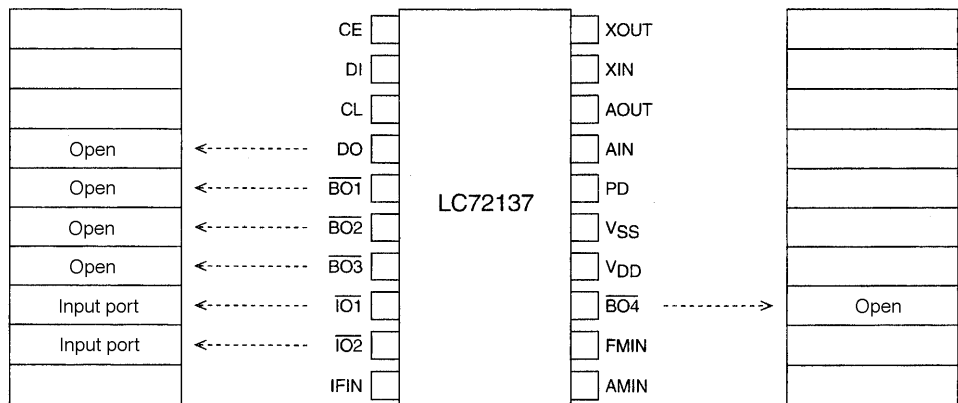
5. Power Supply Pins

A capacitor of at least 2000 pF must be inserted between the power supply  $V_{DD}$  and  $V_{SS}$  pins for noise exclusion. This capacitor must be placed as close as possible to the  $V_{DD}$  and  $V_{SS}$  pins.

6. Note on VCO designing

VCO ( local oscillator ) must keep its oscillation even if the control voltage (  $V_{tune}$  ) goes to 0V. When there is a possibility of oscillation halt,  $V_{tune}$  must be forcibly set to  $V_{CC}$  temporarily to prevent the PLL from being deadlocked. ( Deadlock clear circuit )

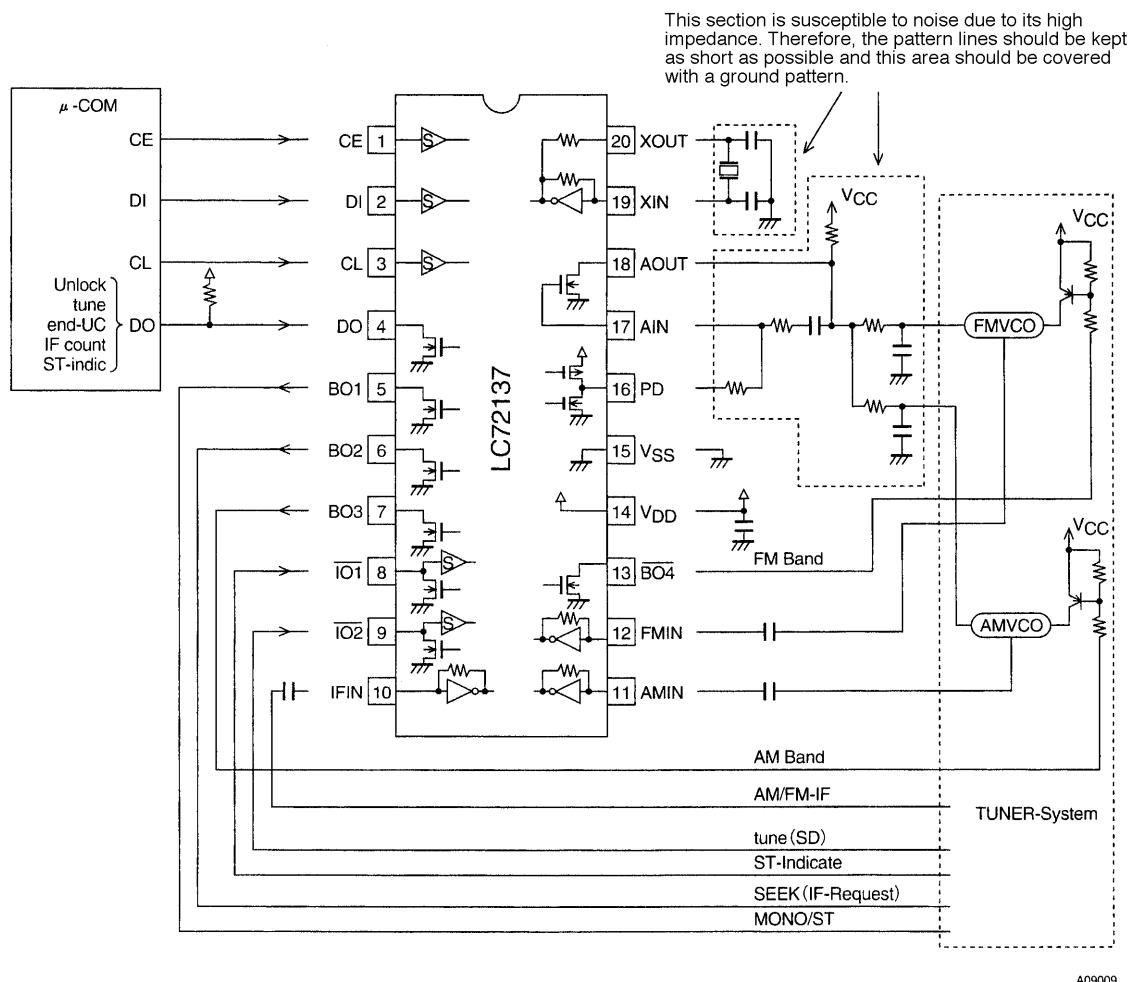
**Pin States at a Power-On Reset**



A09008

## Sample Application System

(Using the MFP20 package)



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